What is claimed is:

1. A method for fabricating a planar inductor in high-performance high-frequency semiconductor circuits, comprising the steps of:

providing a substrate having a first and a second surface, active devices with conductive interconnects being covered by a layer of passivation having been created over the surface of said substrate;

attaching a glass panel to the surface of said layer of passivation;

cutting the first surface of said substrate, said cutting being aligned with a passive region in said second surface of said substrate, said cutting not completely penetrating through said substrate;

removing substrate material from a passive region in the second surface of said substrate, exposing at least one bond pad created on the surface of said passive region on each side of said scribe line; and

cutting said glass panel in alignment with said scribe line.

2. The method of claim 1, said substrate comprising:

a first and a second surface, active devices having been created in or on active surface regions in the second surface of

said substrate, said active surface regions being separated by a passive surface region, a scribe line having been provided across said passive surface region, a layer of insulation having been provided over the surface of said active regions, at least one bond pad having been provided in said passive surface region on each side of said scribe line, a layer of dielectric having been deposited over the surface of said layers of insulation and over said passive surface region separated by said scribe line, at least one bond pad having been created on the surface of said layer of dielectric on each side of said scribe line;

creating at least one planar inductor on the surface of said layer of dielectric on each side of said scribe line, said at least one planar inductor overlying said passive surface region of said substrate;

depositing a layer of passivation over the surface of said layer of dielectric separated by said scribe line;

3. The method of claim 2 wherein at least one layer of interconnect lines is provided in said layer of dielectric, said interconnect lines making electrical contact with said active devices provided in the active regions of said substrate, said interconnect lines further being in contact with said at least one bond pad provided on the surface of said passive region of

said substrate and with said at least one bond pad provided on the surface of said layer of dielectric.

4. The method of claim 2 wherein said at least one inductor created on the surface of said layer of dielectric on each side of said scribe line is connected to said at least one bond pad provided on the surface of said layer of dielectric on each side of said scribe line.

5. A planar inductor in high-performance high-frequency semiconductor circuits, comprising:

a substrate having a first and a second surface, active devices with conductive interconnects being covered by a layer of passivation having been created over the surface of said substrate;

a glass panel attached to the surface of said layer of passivation;

the first surface of said substrate having been cut, said cut being aligned with a passive region in said second surface of said substrate, said cut not completely penetrating through said substrate;

substrate material having been removed from a passive region in the second surface of said substrate, exposing at

least one bond pad created on the surface of said passive region on each side of said scribe line; and

said glass panel having been cut in alignment with said scribe line.

6. The planar inductor of claim 1, said substrate comprising:

a first and a second surface, active devices having been created in or on active surface regions in the second surface of said substrate, said active surface regions being separated by a passive surface region, a scribe line having been provided across said passive surface region, a layer of insulation having been provided over the surface of said active regions, at least one bond pad having been provided in said passive surface region on each side of said scribe line, a layer of dielectric having been deposited over the surface of said layers of insulation and over said passive surface region separated by said scribe line, at least one bond pad having been created on the surface of said layer of dielectric on each side of said scribe line;

creating at least one planar inductor on the surface of said layer of dielectric on each side of said scribe line, said at least one planar inductor overlying said passive surface region of said substrate;

depositing a layer of passivation over the surface of said layer of dielectric separated by said scribe line;

7. The planar inductor of claim 5 wherein at least one layer of interconnect lines is provided in said layer of dielectric, said interconnect lines making electrical contact with said active devices provided in the active regions of said substrate, said interconnect lines further being in contact with said at least one bond pad provided on the surface of said passive region of said substrate and with said at least one bond pad provided on the surface of said layer of dielectric.

8. The planar inductor of claim 5 wherein said at least one inductor created on the surface of said layer of dielectric on each side of said scribe line is connected to said at least one bond pad provided on the surface of said layer of dielectric on each side of said scribe line.

9. A method for fabricating a planar inductor in high-performance high-frequency semiconductor circuits, comprising the steps of:

providing a substrate having a first and a second surface, active devices with conductive interconnects being covered by a layer of passivation having been created over the surface of said substrate divided by a scribe line;

forming a thick layer of a polymer dielectric over the surface of said layer of passivation divided by said scribe line;

creating at least one planar inductor on the surface of said thick layer of a polymer dielectric on each side of said scribe line, said at least one planar inductor overlying said passive surface region of said substrate;

creating at least one bond pad on the surface of said thick layer of a polymer dielectric on each side of said scribe line, said at least one planar inductor overlying said passive surface region of said substrate

attaching an adhesive tape to the surface of said thick layer of a polymer dielectric;

cutting the first surface of said substrate, said cutting being aligned with a passive region in said second surface of said substrate, said cutting partially penetrating through said substrate, said cutting creating a relatively wide cut in said first surface;

wet or dry etching the first surface of the substrate, removing the remainder of the substrate material; and

removing said adhesive tape from the surface of said thick layer of a polymer dielectric.

10. The method of claim 9, said substrate comprising:

a first and a second surface;

active devices having been created in or on active surface regions in the second surface of said substrate;

said active surface regions being separated by a passive surface region;

a scribe line having been provided across said passive surface region;

a layer of insulation having been provided over the surface of said active regions;

at least one bond pad having been provided in said passive surface region on each side of said scribe line;

a layer of dielectric having been deposited over the surface of said layers of insulation and said passive region separated by said scribe line; and

a layer of passivation having been deposited over the surface of said layer of dielectric separated by said scribe line.

11. The method of claim 10 wherein at least one layer of interconnect lines is provided in said layer of dielectric, said interconnect lines making electrical contact with said active devices provided in the active regions of said substrate, said interconnect lines further being in contact with said at least

one bond pad provided on the surface of said passive region of said substrate and with said at least one bond pad provided on the surface of said thick layer of a polymer dielectric.

12. The method of claim 10 wherein said at least one inductor created on the surface of said layer of dielectric on each side of said scribe line is connected to said at least one bond pad provided on the surface of said thick layer of a polymer dielectric on each side of said scribe line.

13. A planar inductor in high-performance high-frequency semiconductor circuits, comprising:

a substrate having a first and a second surface, active devices with conductive interconnects being covered by a layer of passivation having been created over the surface of said substrate divided by a scribe line, said first and second surfaces having been cut through along said scribe line;

a thick layer of a polymer dielectric formed over the surface of said layer of passivation divided by said scribe line;

at least one planar inductor created on the surface of said thick layer of a polymer dielectric on each side of said scribe line, said at least one planar inductor overlying said passive surface region of said substrate; and

at least one bond pad created on the surface of said thick layer of a polymer dielectric on each side of said scribe line, said at least one planar inductor overlying said passive surface region of said substrate.

14. The planar inductor claim 13, said substrate comprising:

a first and a second surface;

active devices having been created in or on active surface regions in the second surface of said substrate;

said active surface regions being separated by a passive surface region;

a scribe line having been provided across said passive surface region;

a layer of insulation having been provided over the surface of said active regions;

at least one bond pad having been provided in said passive surface region on each side of said scribe line;

a layer of dielectric having been deposited over the surface of said layers of insulation and said passive region separated by said scribe line; and

a layer of passivation having been deposited over the surface of said layer of dielectric separated by said scribe line.

15. The planar inductor claim 14 wherein at least one layer of interconnect lines is provided in said layer of dielectric, said interconnect lines making electrical contact with said active devices provided in the active regions of said substrate, said interconnect lines further being in contact with said at least one bond pad provided on the surface of said passive region of said substrate and with said at least one bond pad provided on the surface of said thick layer of a polymer dielectric.

16. The planar inductor claim 14 wherein said at least one inductor created on the surface of said layer of dielectric on each side of said scribe line is connected to said at least one bond pad provided on the surface of said thick layer of a polymer dielectric on each side of said scribe line.